Certificate of Mailing
I hereby certify that on December 20, 2004, this correspondence and any attachments are being deposited with the United States Postal Service as First Class Mail, postage pre-paid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Jeff Beno

PATENT
Atty. Docket No. 38571-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

QIANG SHEN

Application No.: 10/691,078

Filed: October 21, 2003

For: TURBO DECODING

Group Art Unit: 2133

Examiner: Gandhi, Dipakkumar B.

DECLARATION UNDER 37 CFR 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned hereby declares as follows:

1. I am the sole inventor of the invention claimed in the above-referenced patent application (the "Invention").

2. I conceived the Invention prior to May 18, 2000.

3. On or about February 4, 2000, I prepared a formal written disclosure document ("IDF") describing the Invention. The substantive portion of the IDF is attached hereto as Exhibit A.

4. The IDF was reviewed internally by LSI Logic Corporation, my employer at the time and the current assignee of the present patent application, and a determination subsequently was made that a patent application should be filed.

5. It is my understanding that prior to May 18, 2000, the IDF was forwarded to LSI's outside patent counsel, Mitchell Silberberg & Knupp ("MSK"), with instructions that a patent application should be prepared and filed in due course.

6. Subsequently, I was contacted by an attorney from MSK. Thereafter, I promptly cooperated with the attorney: in providing assistance for preparation of an initial draft of the patent application, in reviewing that initial draft, in providing my comments to the attorney, in reviewing the final draft, and in executing and returning the declaration upon completion of such review.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Qiang Shen

Date: 12/08/2004

1. Background

This invention is directly applicable to the 3G cdma mobile phone modem chip development that is under going in the LSI Logic Wireless Design Center.

Turbo codec is needed in 3G cdma mobile communication modem on both mobile station and base station. Since the decoding of turbo code involves interleaving and deinterleaving processes, buffers are needed for that purpose, which comprises most of the memory requirement for turbo decoding. Turbo code is usually implemented for high data rate, which means big memory requirement. So the proper design of the interleaver and deinterleaver in turbo decoder is critical to the size of the modem chip, thus critical to the cost of the LSI product.

In the open literature, the turbo decoder is implemented as follows:

Fig.1. Conventional turbo decoder architecture

INVENTORS:			Lr
Qiang Shen		DATE 02/04/2000	
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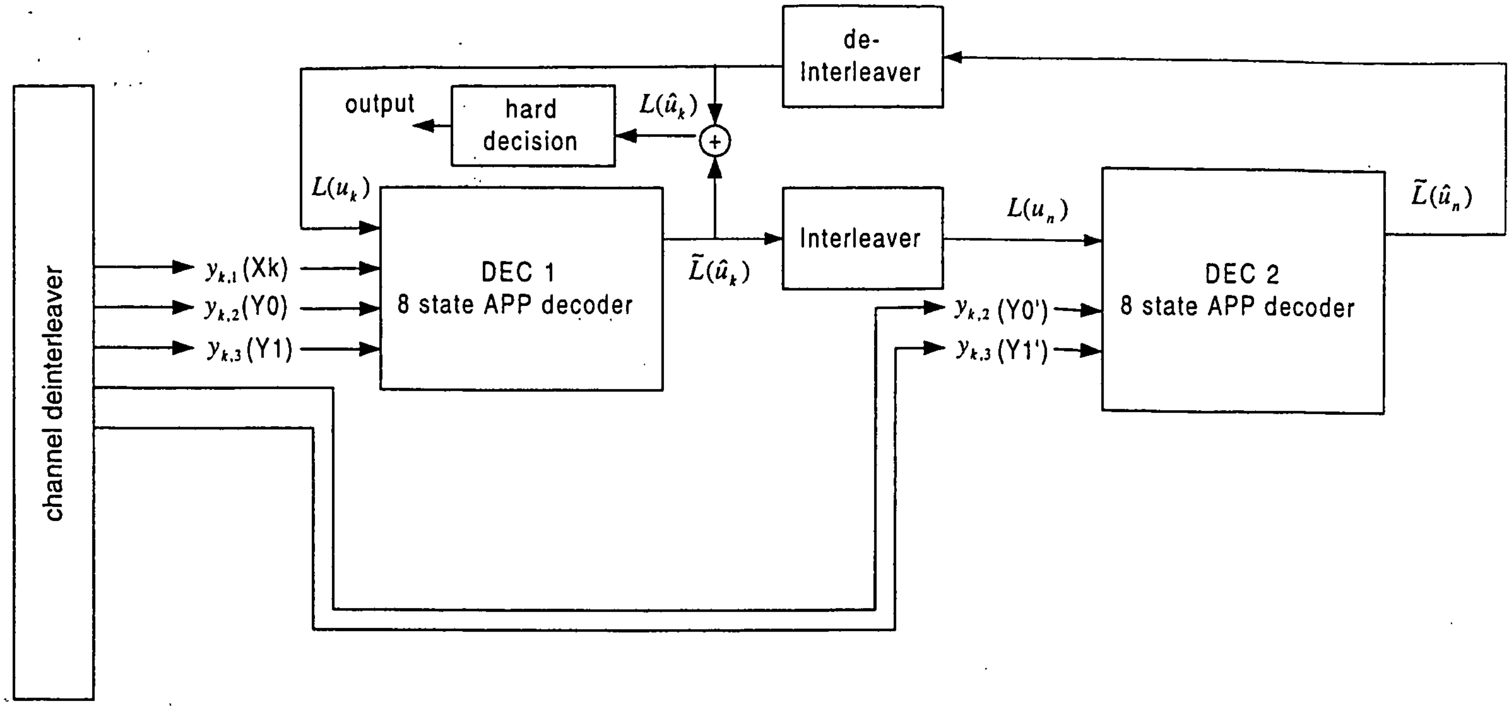
(PRINT) JIAN CUI	(SIGN)	DATE 2/5/00	
(PRINT) Feng Chen	(SIGN)	DATE 2/10/00	



The turbo decoder is composed of mainly two APP decoders, one interleaver and one deinterleave, there are also data available from the channel deinterleaver. A turbo decoder usually operates recursively, which means the output of the DEC2 is fed back to DEC1, and the same process continue for certain times.

As is seen from the figure, there is one interleaver and one deinterleaver between two APP decoders. For IS-2000 supplemental channel of 153.6kbps encoded at ¼ rate, with 8 bits representing each entry of the interleaver and deinterleaver buffer, that means a buffer requirement of

2(banks)x2(buffers)x153.6(kbps)x20(ms)x8(bits)=12Kbyte

2. The invention

INVENTORS:

Qiang Shen DATE 02/04/2000

DATE

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(PRINT)	STASH CZAJA	(SIGN)		DATE	2/5/00
(PRINT)	Feng Qian	(SIGN)		DATE	2/10/00

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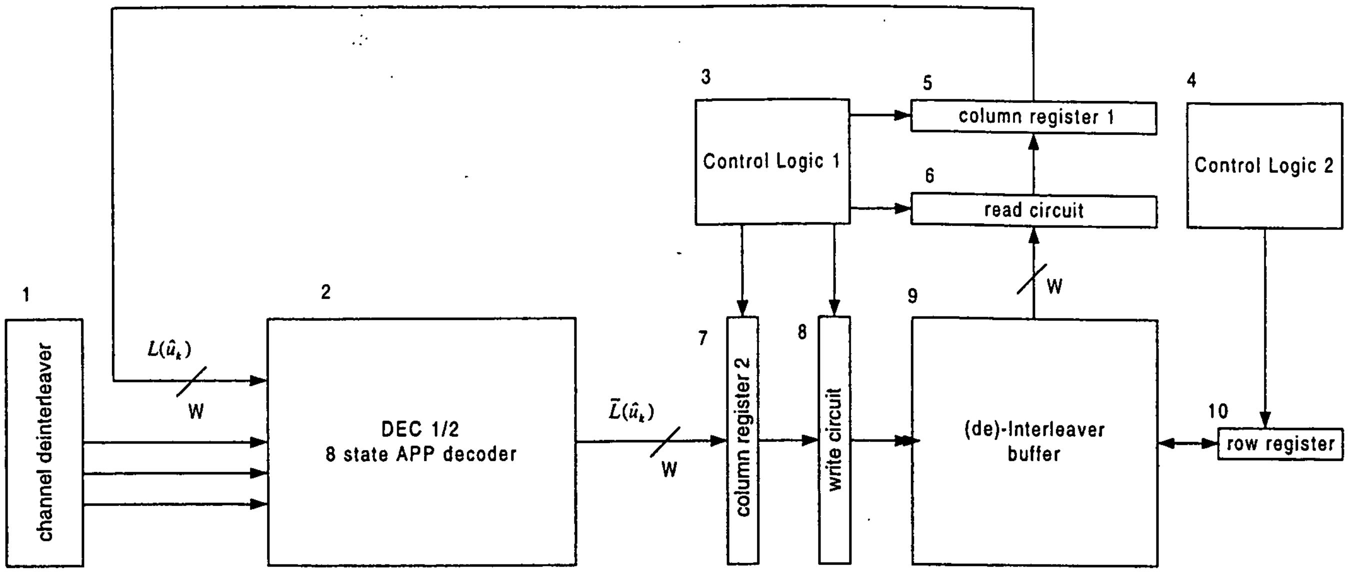
The proposed decoder architecture is shown in fig.2.

Figure 2. Proposed turbo decoder architecture



Here the memory called (de)-interleaver buffer (9) is used for dual purposes, it is used for both interleaving and de-interleaving. The APP decoder (2) will functionally act as DEC1 and DEC2, alternatively. Different hardware configurations surrounding (de)-interleaver are used when the APP decoder is used as DEC1 or DEC2, as will be described in more detail later. All major components required for both modes are shown in figure. 2. Under the same assumption that 8 bits are used to represent soft value, the size of the buffer is

153.6(kbps)x20(ms)x8(bits) = 3 kB

The advantage of the invention is obvious, the memory requirement is reduced from 12Kbyte to 3 Kbytes.

The invention is made possible by exploiting the properties of the turbo code interleaver defined in IS-2000 standard. However, its application is beyond just the is2000 turbo codec. The same architecture applies to

INVENTORS:

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any turbo code that utilizes a matrix interleaver algorithm which can be described as following procedure:

1. Input is written into the matrix row-by-row;
2. The content of each row is permutated in any specific pattern. (It is called column permutation thereafter).
3. Every row as a whole is permutated in any specific pattern. (It is called row permutation thereafter).
4. Output is read out from the matrix column-by-column.

3. Architecture explanation

The indexed blocks in Figure 2 are explained below:

1. Channel deinterleaver stores deinterleaved channel output of the turbo coded symbols.
2. APP decoder is the engine to perform APP (a posteriori probability) decode of RSC1 (recursive systematic code 1) and RSC2 (recursive systematic code 2), alternatively. OK
3. Control logic 1 controls the order the data is read into column register 1 from the (de)-interleaver memory, and performs row permutation of interleaving. It also controls the row permutation at column register 2 and the order of its contents being saved into the (de)-interleaver memory.
4. Control logic 2 controls the read and write of the row register, and the column permutation performed on the row register, as part of the interleaving and deinterleaving operation.
5. Column register 1 hold data from (de)-interleaver memory and output it into the input of the APP decoder in the order controlled by the control logic 1 (3).
6. Read circuit read data from (de)-interleaver memory and save it into the column register 1.
7. Column register 2 hold data from the output of the APP decoder, in the order controlled by the control logic, and when the whole column of data are ready, output them into the (de)-interleaver memory.
8. Write circuit writes the content of the column register 2 into the (de)-interleaver memory, to the column position controlled by the control logic 1.
9. (de)-interleaver memory is a memory space used for both interleaving and deinterleaving, it is conceptually organized as a (Row_number) row and (2^n) coulmn matrix, where Row_number x (2^n) is the smallest integer that is not less than the number of information bits in one turbo encoding data block.
10. Row register saves one row of data from the (de)-interleaver memory, and under the control of the

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control logic 2, put back data into the same row but different position in the (de)-interleaver memory, thus performing column permutation specified by the interleaving and deinterleaving algorithm.

4. Detailed description

4.1. The alternative stages of APP decoder

As shown in both figure. 1 and 2, the APP (*a posteriori* probability) decoder is the core of the turbo decoder. In figure 2, one APP decoder is used for both decoder 1 (DEC1) and decoder 2 (DEC2), and the other hardware including the (de)-interleaver buffer will also be configured accordingly.

For each turbo decoder iteration, the APP decoder is first regarded as the DEC1. And the (de)-interleaver buffer output is the de-interleaved output, its input is the interleaver input. When all data originally in the (de)-interleaver memory have been processed, the output of the APP decoder is also written into the memory, then the whole device is in the second stage at which the APP decoder is regarded as the DEC2.

At DEC2 stage, the (de)-interleaver memory output is the interleaved output, and the buffer input is the de-interleaver input. When the same number of operations are performed, the device finish the DEC2 stage and enter the second iteration of the DEC1 stage, or if it is the end of the iteration, finish the turbo decoding.

4.2. The conceptual organization of (de)-interleaver buffer

At both stages, the (de)-interleaver buffer is always conceptually organized as a matrix of (row_number) rows and (2^n) columns. Parameter n is obtained from the number of bits in each frame for encoding, N_turbo, as shown in following table:

Table 1. IS-2000 turbo code interleaver parameter

Turbo interleaver block size N_turbo	Turbo Interleaver Parameter n
378	4

INVENTORS:	
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570	5
762	5
1,146	6
1,530	6
2,298	7
3,066	7
4,602	8
6,138	8

Parameter row_number = ceil(N_turbo/(2^n)), is the smallest interger that is not less than N_turbo/(2^n).

4.3. DEC1 stage

When the APP decoder is at DEC1 stage, following operations happen:

If the decoder is in the first iteration, then APP decoder takes data directly from the channel de-interleaver buffer, otherwise, it takes certain data from the channel de-interleaver buffer, as well as taking data from the turbo (de)-interleaver buffer. The operation of taking data from channel de-interleaver is not the subject of this invention, thus is not described here. Here we concentrate on the method of obtaining data from the turbo (de)-interleaver buffer.

In the DEC1 stage, both column registers can be bypassed, data are read and written row-by-row, with or without intermediate buffering.

The APP decoder takes data from the turbo (de)-interleaver buffer as de-interleaved data, and puts its output into the same buffer to be interleaved. The output of the decoder will be written into the space previously occupied by the data that have been read out as the decoder input. The following procedure co-ordinates the input and output processes. [illegible]

1. DEC1 input data are saved into the (de)-interleaver memory as described at the DEC2 stage.
2. Data are read out by the read circuit from the (de)-interleaver memory row-by-row, and element-by-element, sequentially.
3. Whenever there are data output from DEC1, it is first saved into the (de)-interleaver memory, at the same sequence as the data is taken into the DEC1.

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Qiang Shen DATE 02/04/2000

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4. The above operation repeats until all N_turbo data is taken into the DEC1 and all N_turbo outputs from the decoder are written into the (de)-interleaver memory. THERE, VE
5. The data in the (de)-interleaver memory is re-ordered according to interleaving algorithm. At this stage all the necessary shuffling within each row is performed. In IS-2000, this is a linear congruential sequence permutation. A row register may be needed for this purpose. ~~Which~~ first fecth a whole row of data from the (de)-interleaver memory, then save each data back in the order controlled by the interleaving column permutation algorithm. For IS-2000, this procedure is described in detail in the attachment: *CBP5.0 project, turbo codec, sec. 2.1.3.*, at row processing stage.

After all the above operations, the decoder enters the DEC2 stage. By that time, the turbo (de)-interleaver buffer holds all the contents that are output of the DEC1 decoder.

4.4. DEC2 stage

When the APP decoder is operating as DEC2 as in figure 1, the following operations are performed:

The APP decoder takes data from the turbo (de)-interleaver buffer as interleaved data, and puts its output into the same buffer to be de-interleaved.

Data in the turbo (de)-interleaver buffer is saved by the previous stage APP decoder as described in the previous section. Data are read from the (de)-interleaver memory, in a column-by-column fashion, first to the column register 1, then into the APP decoder. The row permutation is performed when data is read from the column register 1 to the decoder input. The decoder output is written into the column register 2, before the whole column register 2 is written into the (de)-interleaver memory. The row permutation is also performed before the data of column register 2 is saved into the (de)-interleaver memory. The following procedure describes the coordination of the read and write operation around (de)-interleaver memory.

1. DEC2 input data are saved into the (de)-interleaver memory as described at the DEC1 stage.
2. Data are read out by the read circuit from the (de)-interleaver memory column by column into a temporary column register 1. The order of the column selection is decided by the interleaver algorithm. In IS_2000, it is sequential.
3. Each element in the column register 1 is selectively input into the DEC2, the order of selecting the element is decided by row permutation of interleaver algorithm. In IS-2000, the position is the bit-reverse of the input order, when the bit-reverse value represent the position of a valid data element. A

detailed description of row permutation for IS-2000 is in the attachment: *CBP5.0 project, turbo codec, sec. 2.1.3.*

4. Whenever there are data output from DEC2, it is first saved into the column register 2. The position the data is saved is a reverse operation as those in step 3. A detailed description of this operation for IS-2000 is in the attachment: *CBP5.0 project, turbo codec, sec. 3.1.4. , at column processing stage.*
5. When a column of data is received from the DEC2 output, it is saved into the (de)-interleaver memory, in the same order as the DEC2 input data is taken in step 2.
6. The above operation repeats until all N_turbo data is taken into the APP and all N_turbo outputs from the decoder are written into the buffer.
7. The data in the (de)-interleaver memory is re-ordered according to deinterleaving algorithm. At this stage all the necessary shuffling within each row is performed. In IS-2000, this is a linear congruential sequence permutation. A row register may be needed for this purpose. Which first fecth a whole row of data from the (de)-interleaver memory, then save each data back in the order controlled by the interleaving column permutation algorithm. For IS-2000, this procedure is described in detail in the attachment: *CBP5.0 project, turbo codec, sec. 3.1.4.*, at row processing stage.

After all the above operations, the decoder is ready for the DEC1 stage. By that time, the turbo (de)-interleaver buffer holds all the contents that are output of the DEC2 decoder. The iteration can continue, until the decoding completion, with the a hard decision on the soft value that provided by the APP decoder.

5. Claims (preliminary)

1. The method and apparatus of using one APP decoder and one common buffer to operate alternatively in the dec1 mode and dec2 mode.

2. The method and apparatus of using a smaller intermediate buffer for temporarily storing part of the data before being read into the APP decoder, in accordance with certain operation rules as described.

3. The method and apparatus of performing row permutation on the smaller intermediate buffer as in 2 before sending data into the APP decoder, as part of interleaving operation.

INVENTORS:

Qiang Shen — DATE 02/04/2000

DATE

WITNESS, READ AND UNDERSTOOD BY:

(PRINT) STAN CZAJA	(SIGN)	DATE 2/15/00	
(PRINT) Feng Qian	(SIGN)	DATE 2/16/00	

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4. The method and apparatus of using a smaller intermediate buffer for temporarily storing part of the data from the output of the APP decoder, before being saved into the (de)-interleaver memory, in accordance with certain operation rules as described.

5. The method and apparatus of performing row permutation on the smaller intermediate buffer as in 4 before saving data into the (de)-interleaver buffer, as part of deinterleaving operation.

6. The method and apparatus of performing column permutation on the smaller intermediate buffer and save data back into the (de)-interleaving memory, as part of the interleaving and deinterleaving operation.

7. Attachment

Qiang Shen, "CBP 5.0 Project, Turbo Codec", LSI Logic internal document, Feb. 3, 2000.

INVENTORS:

Qiang Shen	DATE 02/04/2000
	DATE

WITNESS, READ AND UNDERSTOOD BY:

(PRINT)	STANH CHAIA	(SIGN)		DATE 2/5/00
(PRINT)	Feng Qian	(SIGN)		DATE 2/10/00

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Jeff Beno

PATENT
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QIANG SHEN

Application No.: 10/691,078

Filed: October 21, 2003

For: TURBO DECODING

Group Art Unit: 2133

Examiner: Gandhi, Dipakkumar B.

DECLARATION OF PATENT ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Joseph G. Swan, declare that:

1. I am the patent attorney who prepared and filed the above-referenced patent application.
2. I originally received the written invention disclosure from the inventor in this case prior to May 18, 2000.

3. I first contacted the inventor in connection with this case on April 7, 2000. A true and complete printout of the time that I billed in connection with this case (showing such initial contact and my other activities in connection with this case) is attached hereto as Exhibit A.

4. Thereafter, the disclosure was placed into my queue for preparation of patent applications.

5. My standard procedure is to prepare and file patent applications in the order in which they are received. The only exception to this procedure is that any patent applications with approaching statutory bars are prepared and filed prior to their applicable deadlines, generally irrespective of when the corresponding disclosures were received. That is, an application may be taken out turn if patent rights otherwise would be in jeopardy. In addition, other immediately pressing work generally will take precedence over the patent applications in the queue. For example, any Office Action responses with approaching deadlines typically will take precedence over patent applications with no immediate statutory bar.

6. Following my procedures in the preceding paragraph, I began preparation of the above-referenced patent application on July 11, 2000. See Exhibit A.

7. On August 9, 2000, I forwarded the initial draft of the patent application to the inventor, and on September 12, 2000, after incorporating the inventor's comments, I forwarded the final draft of the patent application to the inventor for execution. The patent application subsequently was filed on September 20, 2000. See Exhibit A.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Joseph G. Swan

Date: 12/20/2004

Date	Initials	Name / Invoice Number	Hours	Amount	Description	Matter Number	Index
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07/11/2000	00174	J. SWAN	1.80	495.00	Prepare patent application.	30454-00281	470185
09/28/2000		Invoice=47098	1.80	495.00			
07/12/2000	00174	J. SWAN	1.80	495.00	Prepare patent application; telephone call with	30454-00281	470201
09/28/2000		Invoice=47098	1.80	495.00	client.		
07/14/2000	00174	J. SWAN	2.80	770.00	Prepare patent application.	30454-00281	470221
09/28/2000		Invoice=47098	2.80	770.00			
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07/21/2000	00174	J. SWAN	4.60	1,265.00	Prepare patent application.	30454-00281	470260
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07/24/2000	00174	J. SWAN	1.20	330.00	Prepare patent application.	30454-00281	470270
09/28/2000		Invoice=47098	1.20	330.00			
07/25/2000	00174	J. SWAN	5.80	1,595.00	Prepare patent application.	30454-00281	470272
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07/26/2000	00174	J. SWAN	0.90	247.50	Prepare patent application.	30454-00281	470280
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08/01/2000	00174	J. SWAN	1.80	495.00	Prepare patent application.	30454-00281	471504
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08/07/2000	00174	J. SWAN	1.00	275.00	Prepare patent application.	30454-00281	483098
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08/31/2000	00174	J. SWAN	0.00	0.00		30454-00281	501476
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10/27/2000		Invoice=48981	0.00	0.00	comments; Telephone call with inventor		
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09/12/2000	00174	J. SWAN	0.30	82.50	Preparation of Assignment and Declaration;	30454-00281	497444
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09/20/2000	00174	J. SWAN	0.30	82.50	File patent application.	30454-00281	503848
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